From epitaxy to etch: a unified approach with connected metrology

Christian Kaspari

LayTec AG

LayTec online in-situ seminar

2025-11-13

What do we mean by Connected Metrology?

- Connected Metrology describes
  - the combination of wafer-specific measurements from different processing steps to facilitate a more accurate quantification of complex layer stacks
  - the use of wafer-specific measurements to enable improved accuracy and functionality in downstream processes

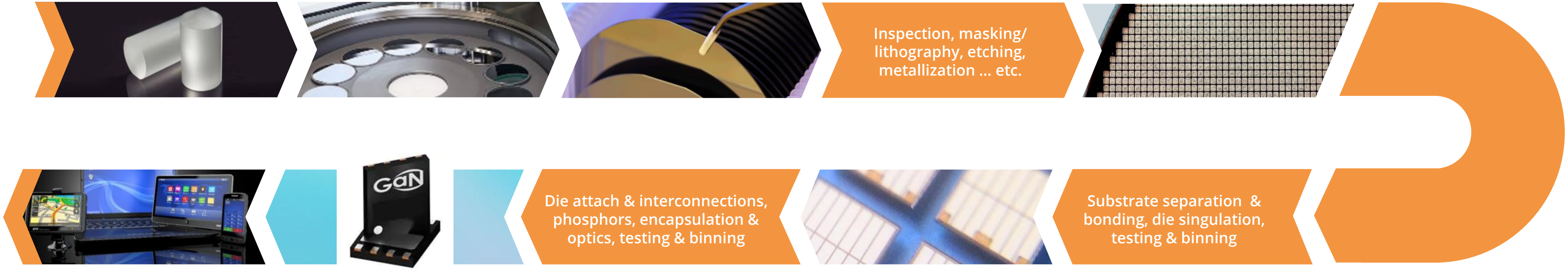
Optical metrology along the semiconductor manufacturing chain

costs — high costs

value — high value generation — maintain or destroy value

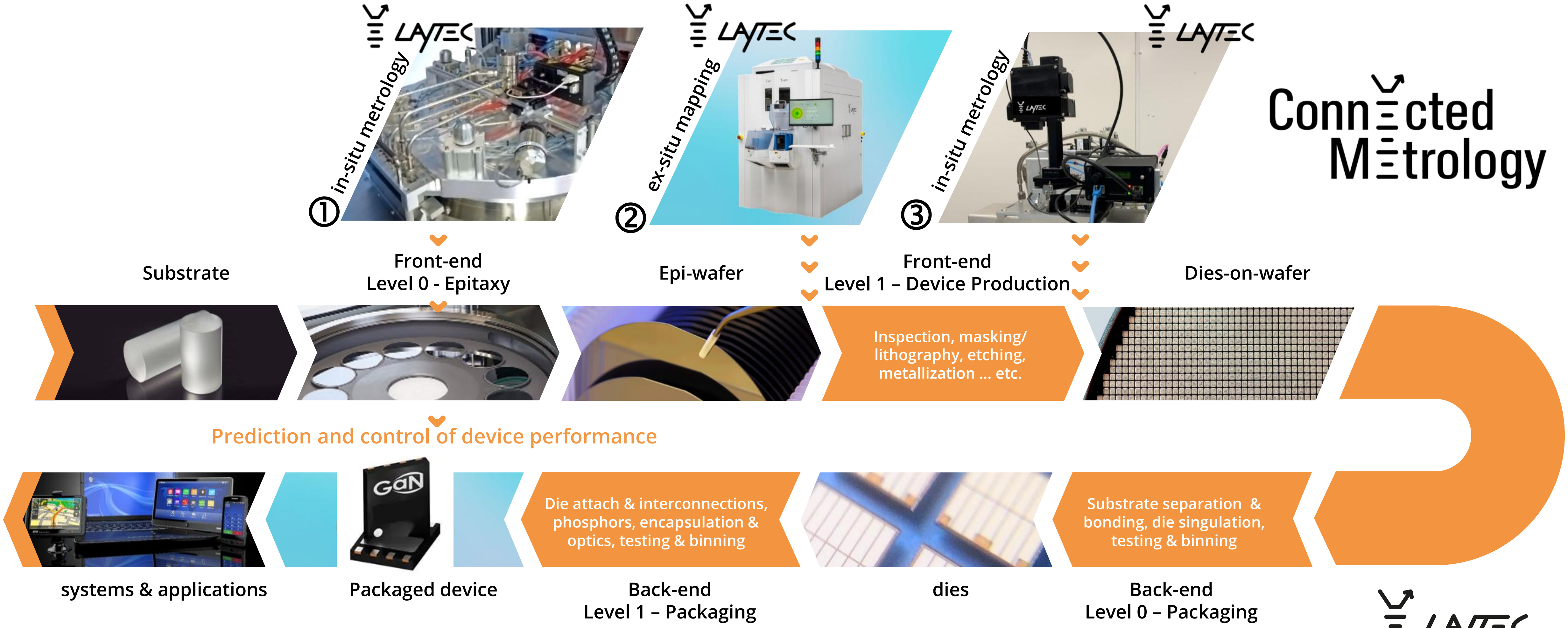
risks — temperature thickness composition — unknown uniformity — wrong etch stop

Substrate | Front-end Level 0 - Epitaxy | Epi-wafer | Front-end Level 1 – Device Production | Dies-on-wafer



systems & applications | Packaged device | Back-end Level 1 – Packaging | dies | Back-end Level 0 – Packaging

Optical metrology along the semiconductor manufacturing chain

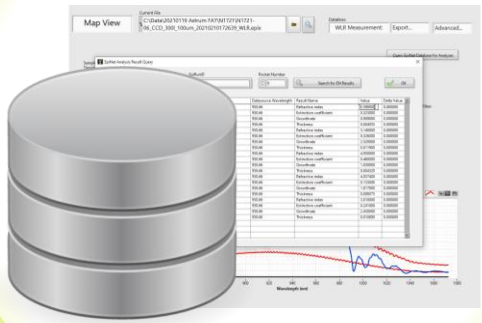


LayTec “Metrology Ecosystem”

***EpiCurveTT*:**
in-situ measured layer thickness
and other layer properties

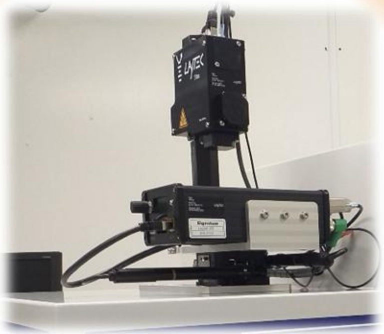
In-situ metrology during MOCVD

Database of
measured data



Wafer mapping

***EpiX*:**
spatial variation
of layer properties



In-situ metrology during
plasma etching

***Etchpoint* and *TRIton*:**
end point detection based
on <u>actual</u> layer thickness

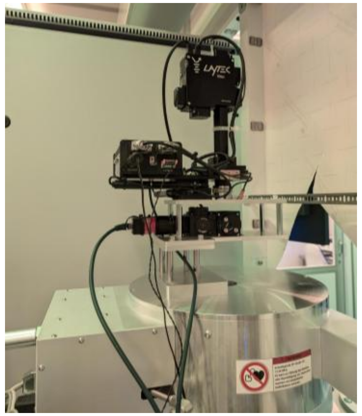
- The same wafer is measured 3+ times
- The amount of information increases
- and is combined for improved analysis in downstream processes

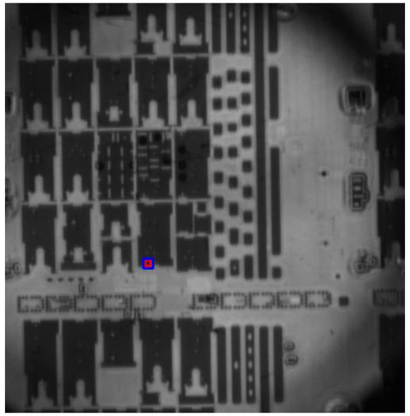
MEMBER OF THE NYNOMIC GROUP

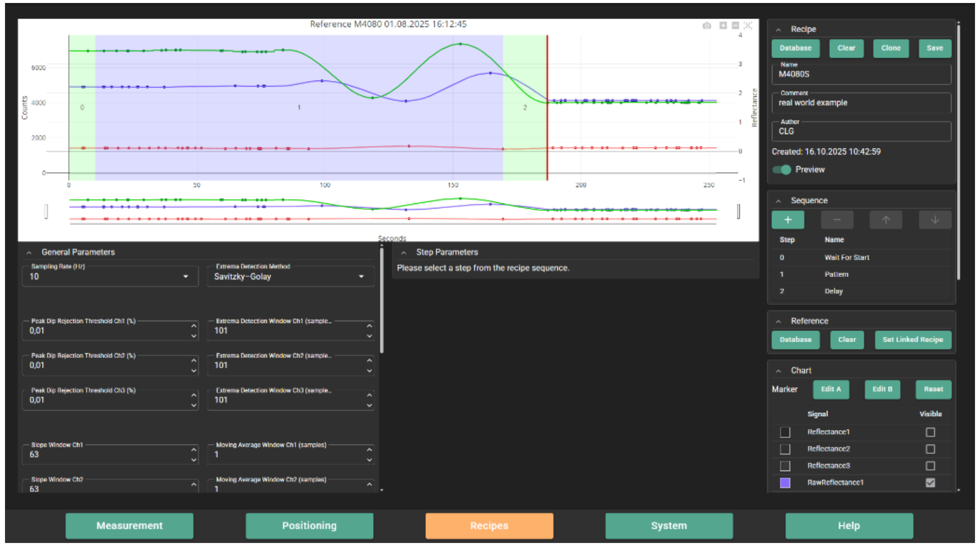
What do we mean by Connected Metrology ?

- Connected Metrology describes
  - the combination of wafer-specific measurements from different processing steps to facilitate a more accurate quantification of complex layer stacks
  - the use of wafer-specific measurements (actual layer thickness) to enable improved accuracy and functionality in downstream processes

Application: Epi to Etch for reflectance-based EPD





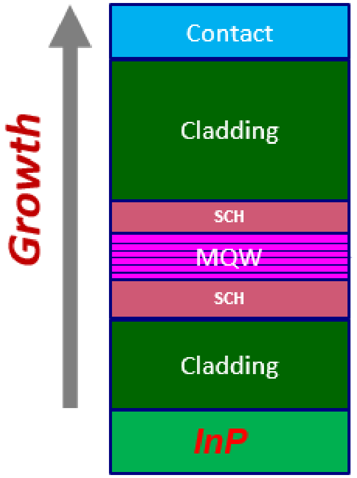


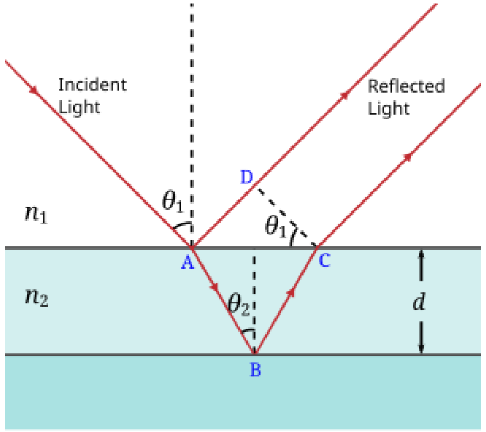
- **LayTec TRIton with EtchNet SW package**
- Reflectance based interferometry tool
- Compatible with many plasma etch tools
- Multiple wavelengths … incl. UV
- Camera for pattern recognition
- Automated end-pointing algorithms
- Simulation and modelling software SimulyzR

MEMBER OF THE NYNOMIC GROUP

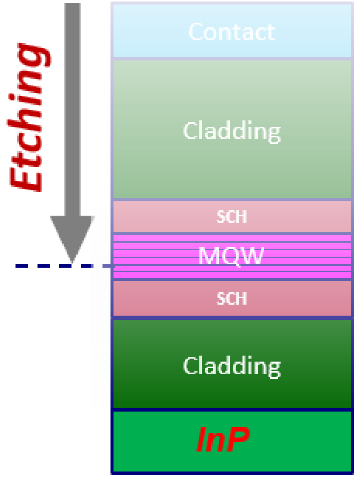
Growth and etching of InP-based laser structures

Schematic layer stack

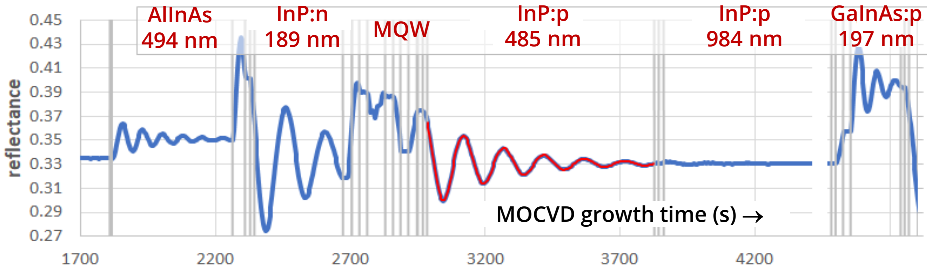




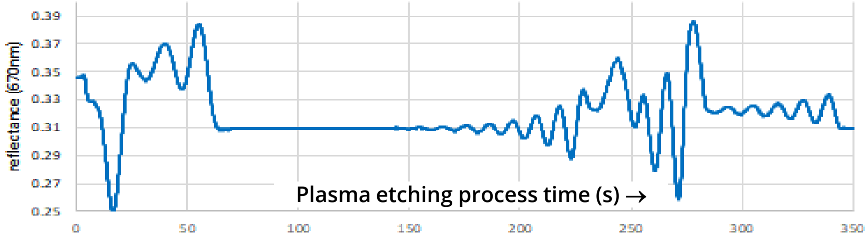
- In-situ metrology during epitaxy
  - Measure growth rate and layer thickness
  - Interface detection by communication with epi tool
  - Thickness information can be used for controlling etching process
- In-situ metrology during etching
  - Interfaces must be detected based on optical signal
  - Etch rate can be measured
  - (Residual) thickness can be calculated



Reflectance data during growth



Reflectance data during etching



MEMBER OF THE NYNOMIC GROUP

It's all about the layer stack

Wavelength

- Wavelength sequence according to TRIton LED, e.g.:
  - LED1: 340nm
  - LED2: 670nm
  - LED3: 405nm

Materials

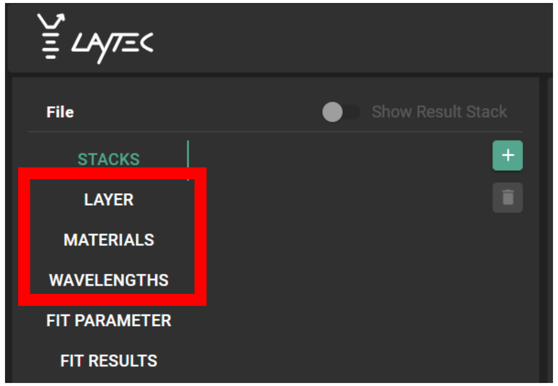
- Database Material
  - Composition
- n,k constants of material
  - n,k
- n,k Multi-WL Material
  - n,k for each wavelength

Layers

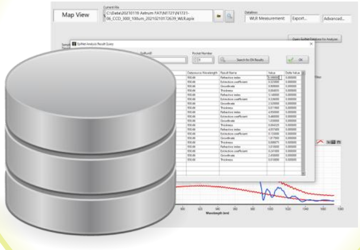
- Layer (Rate/Duration)
  - ID
  - Material
  - Temperature
  - Start time offset
  - Duration
  - Thickness
  - Rate
- Layer (Start/Stop)
  - ID
  - Material
  - Temperature
  - Start Time offset
  - End time offset
  - Start thickness
  - End thickness
- Macro Layer
  - ID
  - Number of repeat
  - Layer stack

Stack

- New layer stack:
  - ID
  - Layer sequence
  - Alpha correction
  - Virtual interface:
    - AbsR
    - Phi



Database of measured data

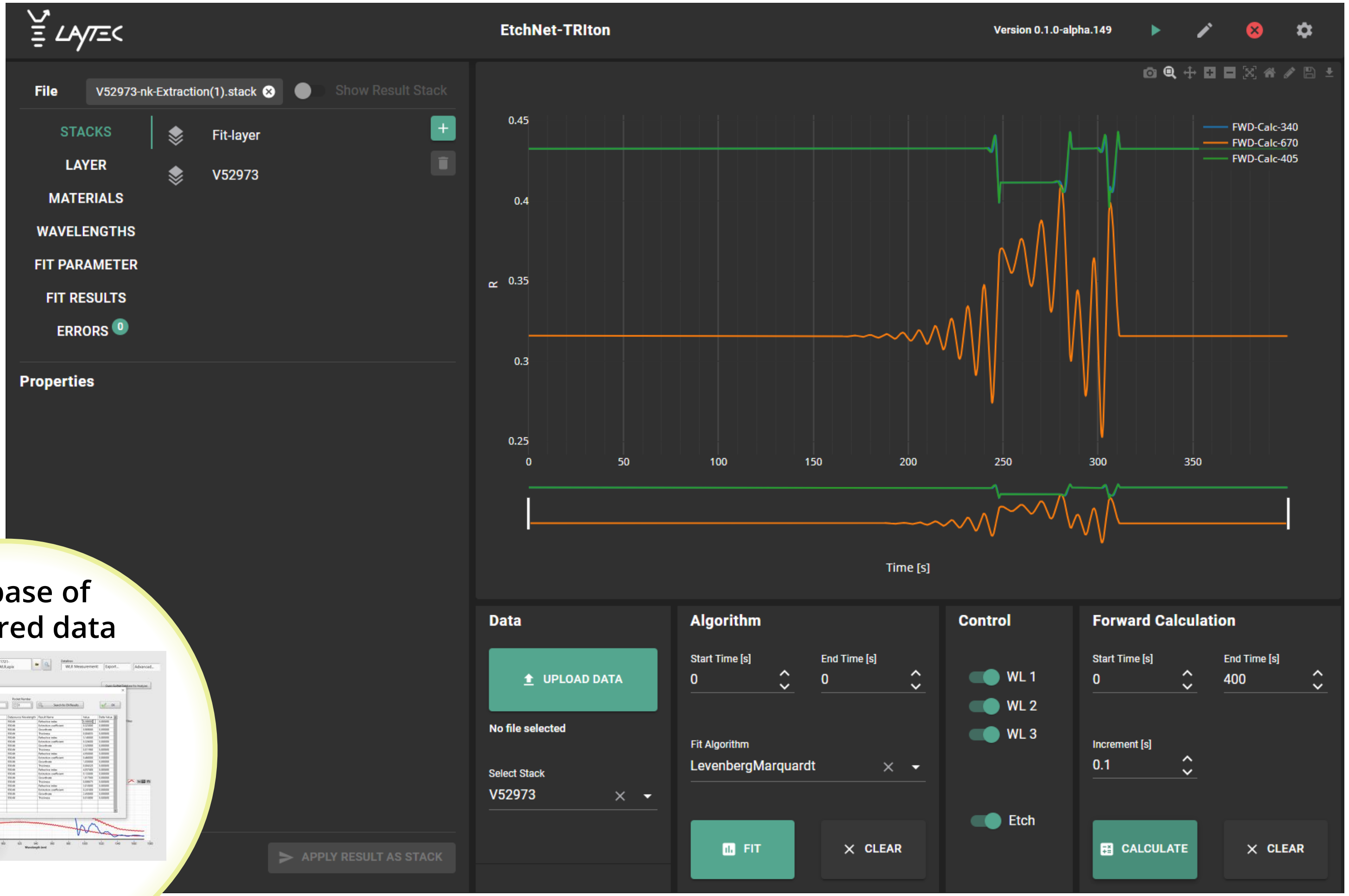


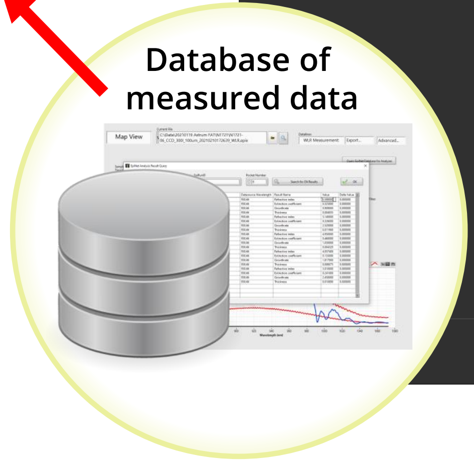
- Stack definition constant for distinct recipe
- Properties are wafer-specific!
- LayTec SimulyzR SW package helps to handle this complexity

MEMBER OF THE NYNOMIC GROUP

SimulyzR – forward calculation of layer stack

- Expected etch-transient is calculated based on pre-defined layer stack
- Known layer thickness from epitaxy can be helpful for a precise stack definition

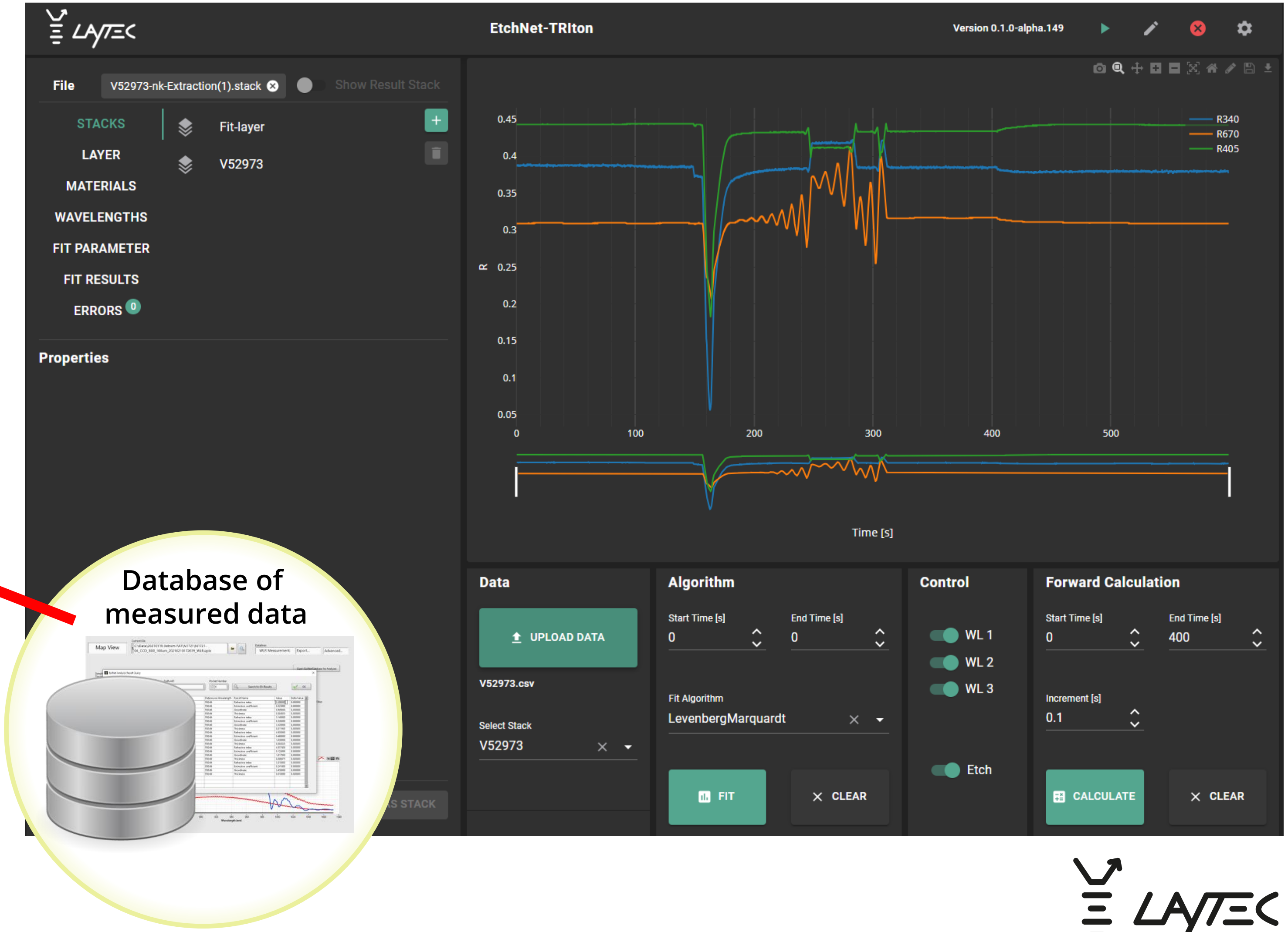




MEMBER OF THE NYNOMIC GROUP

SimulyzR – recipe engineering using etch data

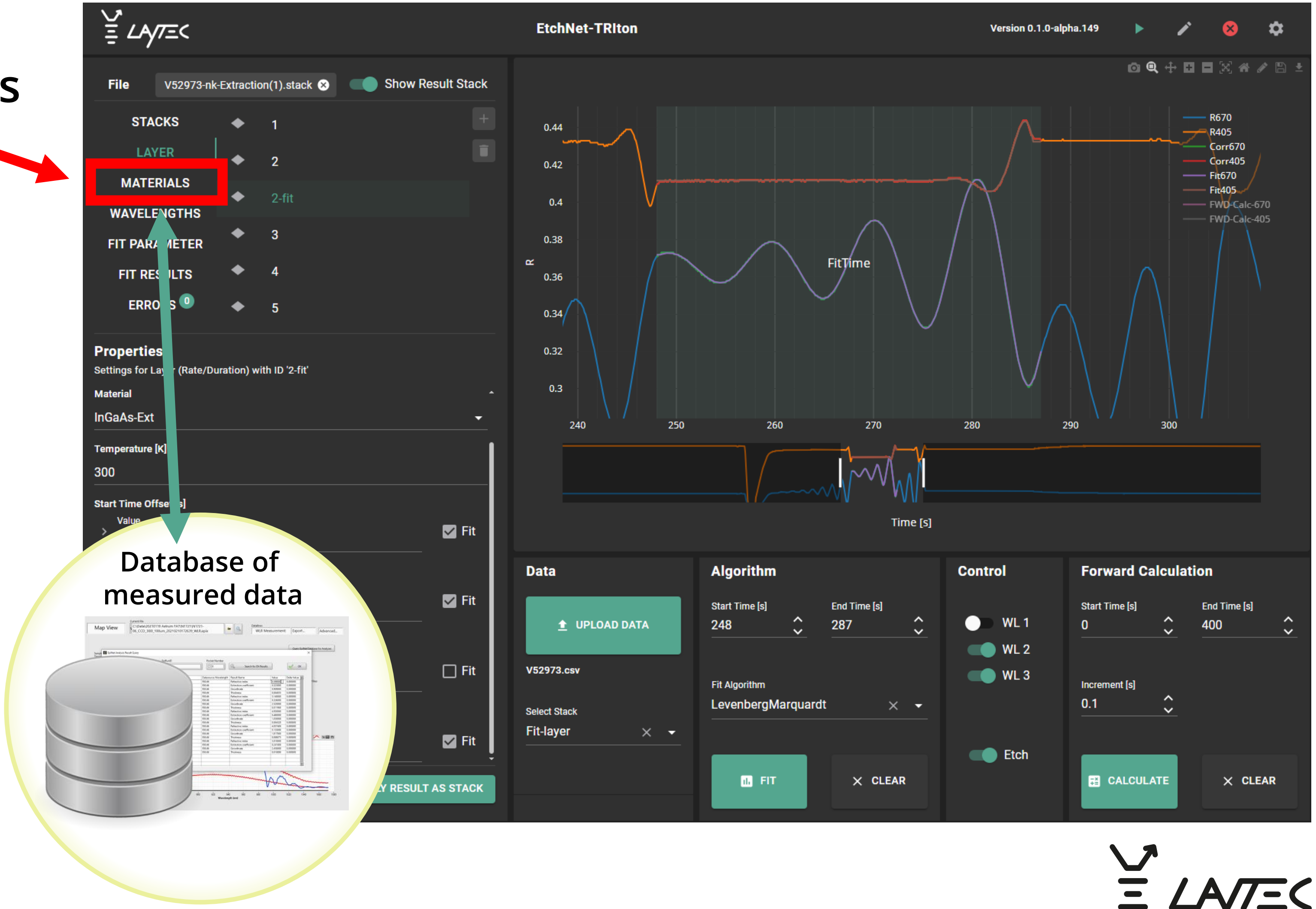
- Measured etch data is imported
- Layers can be fitted and updated in stack
- Known layer thickness from epitaxy can add additional information for fit
- Used to engineer suitable automated endpoint recipes for EtchNet



MEMBER OF THE NYNOMIC GROUP

SimulyzR – improved n,k database

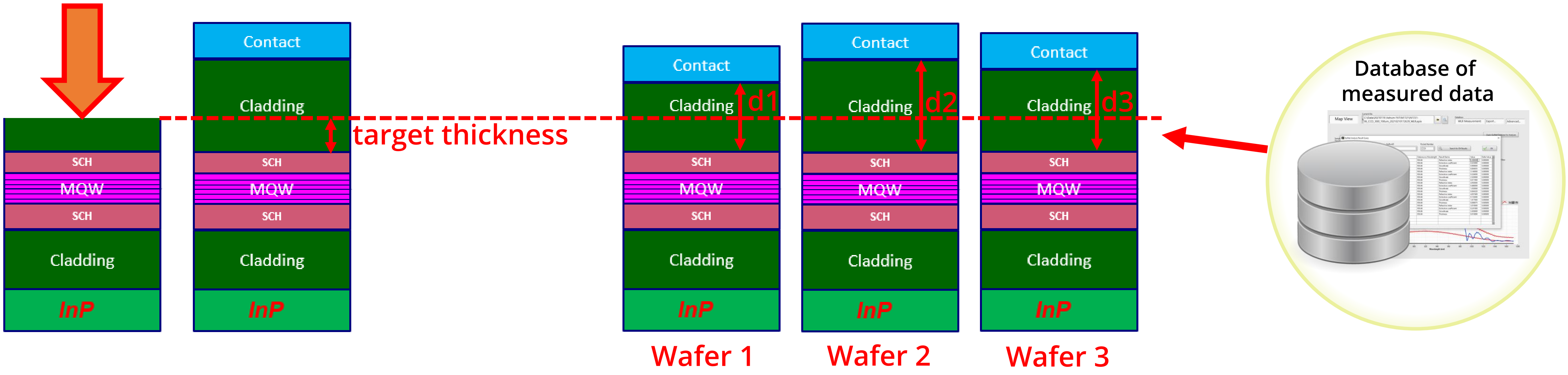
- Fit obtains n,k for etch process
- Not the same as for growth process, lower T!
- Known layer thickness from epitaxy improves accuracy of n,k fit
- Update n,k database for etch recipes



MEMBER OF THE NYNOMIC GROUP

Example: Shallow ridge etch process (Ridge Waveguide laser)

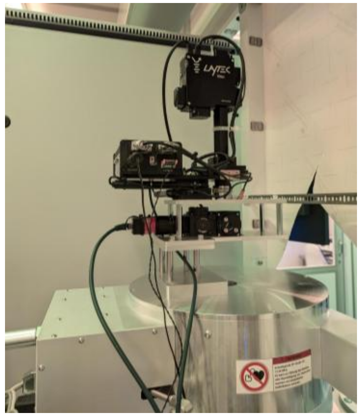
Assumed (exaggerated) variation of p-cladding:



- Use individual p-cladding thicknesses d1, d2 d3 from epitaxy (EpiNet Analysis) via database
- Use this information for wafer-specific individual etch stop
- Etch process with improved w2w uniformity

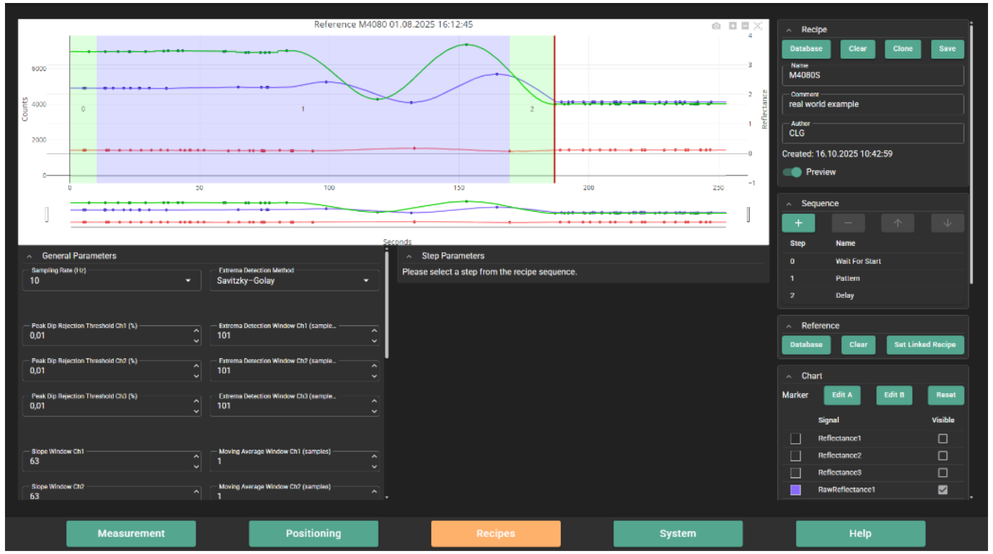
MEMBER OF THE NYNOMIC GROUP

Epi to etch for reflectance-based EPD with Connected Metrology



Wafer-specific layer stack quantification from epitaxy (& mapping) enables

- Advanced simulation and prediction of etch transients
- More accurate and reproducible end-pointing



MEMBER OF THE NYNOMIC GROUP

Knowledge is key

www.laytec.de

LAYTEC
MEMBER OF THE NYNOMIC GROUP