Connected Metrology® for InP photonics

Wafer-specific data from EpiCurve® TT, EpiX® and TRIton® to enable high-yield InP device production for AI-scale optical interconnects

Executive summary

AI chips do not scale on compute transistors alone. Training clusters and AI factories increasingly depend on high-bandwidth, low-latency and power-efficient optical links. As 800G and 1.6T optics, silicon photonics and co-packaged optics move optical engines closer to switch ASICs and accelerators, InP lasers, photodiodes and related optoelectronic devices become strategic manufacturing assets rather than niche components.

For InP wafer and device manufacturers, the manufacturing challenge is therefore changing: It is no longer sufficient to perform a nominal epitaxy run and verify a few post-process samples.

Complex multi-layer InP stacks must be controlled wafer by wafer, across epitaxy, mapping and plasma etching, while volumes and cost pressure increase. In frontend, epitaxy creates high value; dry etching can preserve that value - or destroy it if the endpoint is wrong.

Connected Metrology®, as used here, means the wafer-specific combination of measured data during epitaxy with EpiCurve® TT, post-epi wafer mapping with EpiX®, and plasma-etch monitoring with TRIton®. Linked by the wafer ID in a common data environment, these measurements create a process-control architecture: upstream data provide prior knowledge for downstream steps, and downstream results close the loop for root-cause analysis, run-to-run control and yield improvement.

Wafer-specific data flow

1. Epitaxy EpiCurve® TT	2. Wafer mapping EpiX®	3. Plasma etch TRIton®
In-situ pyrometry, reflectometry and deflectometry. Measures temperature, growth rate, layer thickness, composition and wafer curvature/bow.	Ex-situ full-wafer PL/bow maps. Quantifies luminescence, composition, and spatial uniformity down to die-level decisions.	In-situ multi-wavelength reflectometry. Detects interfaces, extracts etch rate and residual thickness, and sends automated endpoint signals.

Connected Metrology® turns the question from “Did this wafer follow the recipe?” into “What is the actual wafer-specific layer stack, spatial distribution and residual thickness right now – and how should the next process step adapt?”

Why InP photonics raises the metrology threshold

AI infrastructure is creating a manufacturing pull for high-speed optical interconnects. Industry sources point to the rapidly growing demand for optical transceivers with 800G and higher data rates, the emergence of CPO and optical I/O interfaces, and the growing interest in high-quality lasers. InP is central because electro-absorption modulated lasers (EMLs), continuous-wave (CW) laser sources and high-speed photodiodes depend on III-V epitaxy and frontend processing with tight dimensional and material tolerances.

The technical consequence is straightforward: device performance is determined by a stack of coupled variables. Epitaxy sets layer thickness, composition, strain and curvature. Wafer mapping reveals spatial non-uniformity that a single in-situ trace cannot fully describe. Plasma etching defines critical residual layers, ridge height, contact-layer preservation, optical coupling and electrical resistance. Each step has its own metrology, but the device sees the integrated history of the wafer.

Wafer-specific data flow

Process step	Main value created	Dominant risk	Connected response
Epitaxy	High-value InP heterostructure with MQWs, claddings, contact layers and composition targets.	Run-to-run and wafer-to-wafer deviations in temperature, thickness, composition, strain and bow.	Use EpiCurve® TT to capture actual layer growth, interface positions and wafer behavior in real time.
Post-epi mapping	Full-wafer qualification and release knowledge.	Unknown spatial distribution; center-point data hide local excursions.	Use EpiX® to map thickness, composition, PL parameters and bow, then feed maps back to epi and forward to etch.
Dry etch	Device geometry and residual layers that preserve electrical and optical function.	Wrong endpoint, over-etch, under-etch, etch-rate drift, non-uniformity and batch-to-batch variation.	Use TRIton® for direct, reflectance-based endpointing instead of recipe time; even without upstream wafer data, TRIton® improves etch accuracy, while Connected Metrology® further refines the endpoint using the actual measured layer stack.

The Connected Metrology® architecture

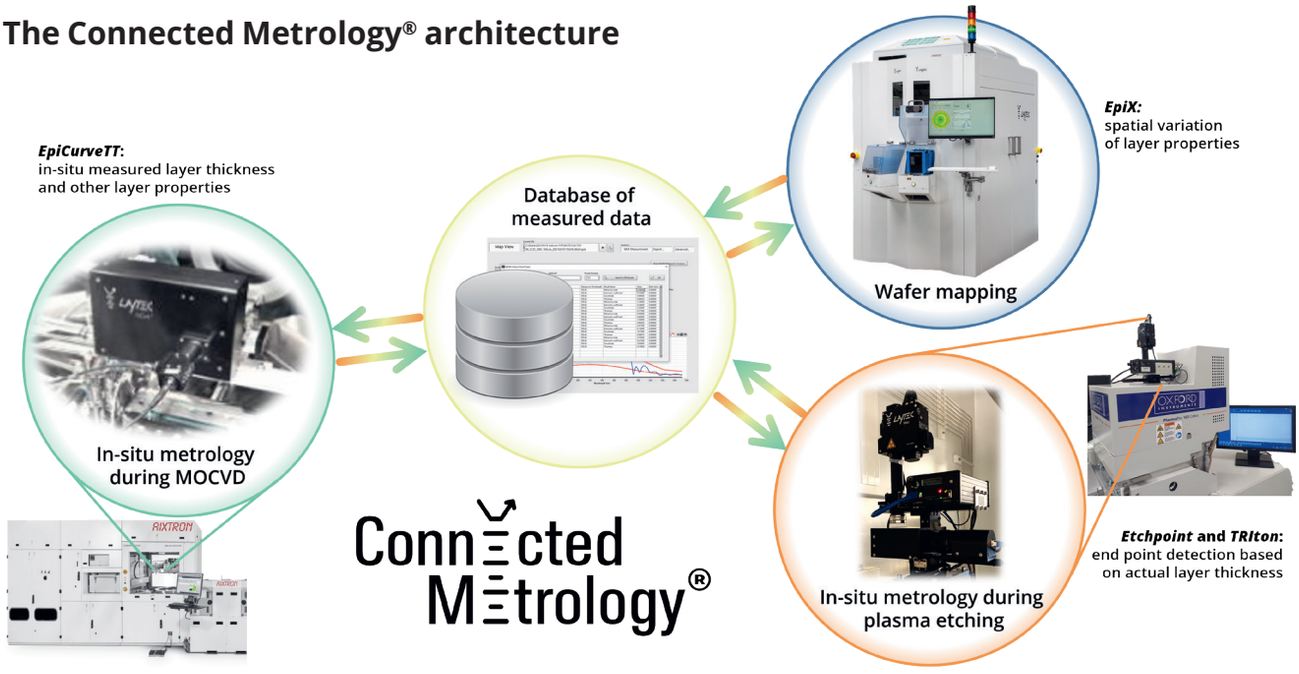

Fig. 1: LayTec Metrology Ecosystem: Connected Metrology® combines wafer-specific in-situ epitaxy data, post-epi wafer mapping and in-situ etch monitoring in one metrology ecosystem.

The architecture is deliberately wafer centric. The same wafer is measured three or more times along the frontend chain. The amount of information increases with each step and is combined for improved analysis in downstream processes. This constitutes a unified metrology ecosystem in which in-situ epi data, post-epi maps and in-situ etch data are linked by wafer ID:

- EpiCurve® TT during MOCVD combines wafer curvature measurements with emissivity-corrected pyrometry and multiple-wavelength reflectance. For InP lasers it provides real-time growth-rate and thickness information, plus wafer bow/curvature and temperature context.

- EpiX® adds spatial information: UV-VIS-NIR white light reflectance, photoluminescence and optional bow mapping. For InP optoelectronics this means full-wafer maps of PL peak wavelength, intensity and other luminescence parameters linked to composition and layer quality.
- TRIton® brings the wafer history into plasma etch. Multi-wavelength reflectometry supports interface detection, etch-rate extraction, residual-thickness calculation and within-layer endpointing. Algorithms can be tailored to the stack and can compensate tool communication delays.

Physics first, analytics second: raw optical traces should first be interpreted with physical thin-film models. The resulting high-level parameters – thickness, composition, curvature, etch rate, residual thickness and uniformity – are then well suited for SPC and future machine-learning models without breaking physical consistency.

InP laser case: etching into a known structure

An InP edge-emitting laser is a coupled optical, electrical and mechanical layer system, not just a nominal thickness stack. InP claddings, AlInAs/AlGaInAs confinement layers, MQWs and GaInAs contact layers must be grown with controlled thickness, smooth morphology, interface position, composition and strain. Thickness sets optical mode position and etch targets; quaternary composition sets bandgap, emission wavelength and band offsets; strain reveals lattice mismatch and residual stress. Production metrology must therefore identify both the actual interfaces and the material properties of the wafer. During MOCVD, EpiCurve® TT tracks thin-film interference to extract growth rate, layer thickness and interface positions as well as any undesired surface roughness; curvature adds the wafer stress/strain response. For quaternary InP-based layers, composition is not a reflectance-only parameter: thickness, optical constants, strain and alloy content are coupled, and a single in-situ trace gives only a partial view. EpiX® closes this gap after growth. Its PL maps provide wafer-scale access to bandgap and composition of critical active/confinement layers. Reliable production-level composition control therefore comes from combining in-situ reflectance, in-situ curvature and ex-situ PL mapping.

Why this matters for hybrid InP-on-silicon photonics

In hybrid InP-on-silicon photonics, this wafer-specific knowledge is essential. A very thin InP contact/conduction layer may be required for evanescent coupling and electrical conduction; etching too deep increases series resistance, while leaving too much material compromises the optical/electrical design. TRIton® uses the measured stack downstream: the plasma etch travels through the grown sequence in reverse, so a time-inverted epi reflectance trace previews the etch signal. The real trace differs in wavelength, temperature and etch rate, but the interface sequence remains recognizable. TRIton® is the navigation system through the layer stack. Integrated algorithms can then detect interfaces, extract etch rate, calculate residual thickness and specific endpointing algorithms stop at the right depth based on the wafer in the chamber rather than recipe time alone.

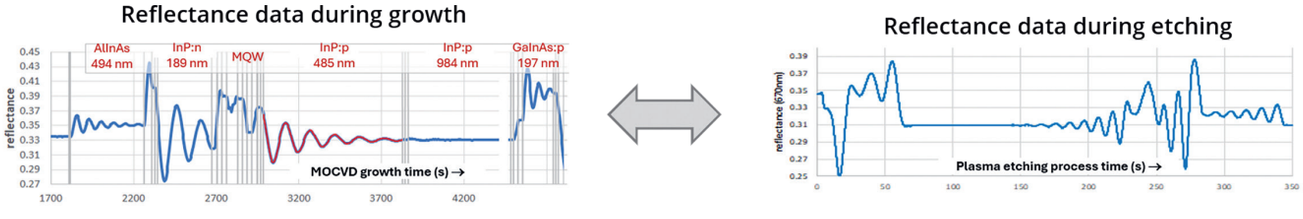

Fig. 2: Connection between growth and etch reflectance: Time-inverted epitaxy reflectance provides a wafer-specific preview for plasma etching, enabling endpoint control against the actual grown layer stack.

Production-level control requires more than a correct nominal recipe. It requires metrology that is accurate and stable enough to distinguish real wafer variation from measurement noise. This is particularly important for InP-based laser stacks containing quaternary AlInGaAs or InGaAsP layers. In-situ reflectance provides thickness, interface and growth-rate information, but composition access can be incomplete when several quaternary layers contribute simultaneously to the optical response. EpiX® PL mapping adds a complementary, composition-sensitive wafer map, while in-situ curvature adds strain information. Only the combination of in-situ reflectance, in-situ curvature and ex-situ PL mapping provides a production-relevant view of actual layer composition, thickness and strain. The same principle carries into etching: once the wafer-specific stack is known, TRIton® endpointing can use real-time reflectance to compensate etch-rate variation and stop at the intended residual layer.

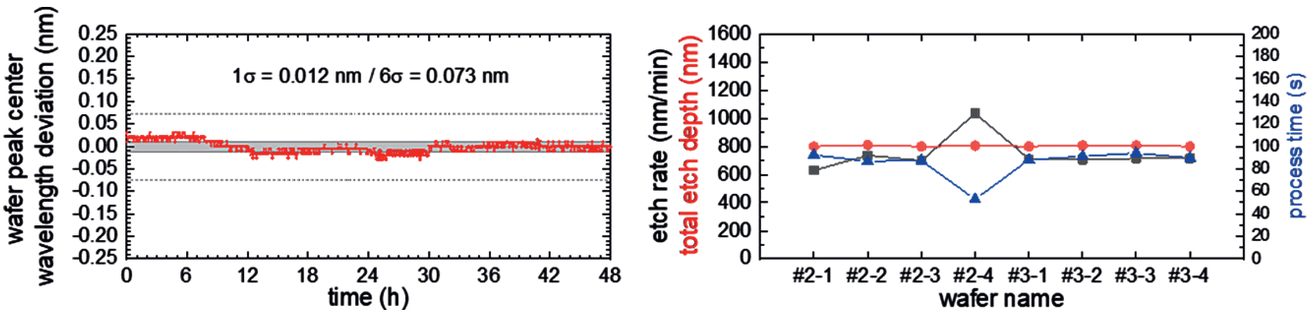

Fig. 3: Accurate measurements enable production-level control: Panel A – Long-term EpiX® PL measurement stability demonstrates that wafer mapping can provide repeatable, composition-sensitive data for InP-based layer stacks, supporting wafer release, feedback to epitaxy and composition control of critical quaternary layers. Panel B – TRIton® reflectance-based endpointing converts real-time optical information into process control: when the etch rate is deliberately varied, the endpointing algorithm adapts the etch time and keeps the final etch depth constant. Together, the two examples illustrate the central principle of Connected Metrology® : reliable measurement data transform wafer-specific variation into controllable process parameters.

Connected Metrology® element	What it adds	Manufacturing value
EpiCurve® TT reflectance measures wafer-specific growth rate, thickness and interface positions during MOCVD.	Etch targets originate from the measured stack, not the nominal recipe.	Less ambiguity at thin residual layers and device-critical interfaces.
EpiCurve® TT curvature plus EpiX® PL mapping combine strain/lattice-mismatch data with wafer-scale PL peak wavelength.	Thickness, strain and bandgap/ composition are separated with complementary physical observables.	Production-level access to composition variations in quaternary InP layers.
Time-inverted epi reflectance provides a preview of the plasma-etch trace; shorter wavelengths improve interface visibility.	TRIton® uses prior layer data while detecting the real-time etch signal.	More confidence when stopping before, at or inside a target layer.
Endpointing trials with varied etch rate kept total etch depth essentially constant.	Endpointing compensates process drift.	Batch-to-batch consistency, including faster chemistries where time-based control is too risky.

What changes in day-to-day engineering

- Endpoint recipes can be built from wafer-specific thickness, strain and PL-derived composition data, then refined with etch-through baselines, extrema tracking and pattern recognition.
- EpiX® maps become more than release data: PL peak shifts and composition gradients can help define engineering limits, regional binning and etch assumptions.
- Epi, mapping and etch engineers can debug the same wafer history instead of comparing disconnected logs, center-point measurements and late ex-situ inspection results.
- SPC shifts from tool-level averages to material-aware parameters: thickness, curvature, strain, PL peak, composition, etch rate and residual thickness.

Value for manufacturers: technical control with business consequences

Connected Metrology® is not a single sensor upgrade. It is a wafer-history layer for the InP frontend. For engineers, the value is better visibility and a more deterministic process. For decision makers, the value is the ability to ramp volume while moving yield learning upstream – from late-stage scrap, manual troubleshooting and conservative process margins to wafer-specific process data.

Engineering outcomes	Operational outcomes
Actual stack data, strain history and PL-derived composition maps are used in downstream analysis, reducing ambiguity in root-cause investigations.	High-value epi wafers are protected during etch, lowering the probability of avoidable scrap.
Full-wafer maps expose local non-uniformity in thickness, PL wavelength and composition-sensitive bandgap, enabling die-level pass/fail or targeted process feedback.	Qualification cycles shorten because destructive methods become (less often used) validation tools rather than routine discovery tools.
Endpointing can adapt to etch-rate variation and tool delays, improving transferability across batches and chambers.	Higher process capability supports customer ramps in 800G/1.6T optics and next-generation optical I/O supply chains.
Physics-based parameters can feed SPC and machine-learning models without losing the link to thin-film optics, strain and PL-derived composition.	A common wafer-ID data foundation improves traceability for internal quality systems and external customer audits.

A practical deployment path

1. Establish a centralized LayTec measurement database all EpiCurve® TT, EpiX® and TRIton® tools connect to where data can be linked based on the specific wafer IDs. Define the critical parameters for each InP product family: layer thickness, PL-derived bandgap/composition, strain/curvature, bow, etch target, residual layer and device-test correlation.

2. Equip key MOCVD processes with EpiCurve® TT and establish fit recipes for the layer stack. Use destructive or high-resolution ex-situ methods only to validate model accuracy during development and transfer.

3. Deploy EpiX® maps to measure spatial thickness, PL peak wavelength, composition-sensitive bandgap/luminescence distributions and optional bow. Use in-situ epi results as starting values for 2D fits and convert maps into engineering limits or die-level decisions.

4. Build TRIton® endpoint algorithms from etch-through baselines, multi-wavelength traces and prior epi thickness. Validate with SEM/profilometry, include tool delay compensation, then lock production recipes.

5. Close the loop through SPC: feed EpiX® uniformity and composition maps back to epi, use the combined epi/mapping data in etch decisions, and correlate the full wafer history with final device performance.

Conclusion

For InP photonics in next-generation AI chips or datacom, the enabling potential of Connected Metrology® is wafer-specific manufacturing intelligence. It allows manufacturers to know the actual layer stack during growth, quantify the spatial and composition-sensitive distribution before release, and endpoint plasma processes against the wafer that is actually in the chamber. The combination of in-situ reflectance, in-situ curvature and ex-situ PL mapping is the technical foundation for scaling InP devices with tighter specs, higher yield and greater confidence.

The “Connected Metrology” approach

The LayTec Connected Metrology® ecosystem enables improved process control characterizing complex layer stacks along the manufacturing chain. In a typical frontend production line, wafers are typically measured multiple times. Using LayTec systems in all of these process steps bears the potential to forward and share the respective analysis data from each step to the subsequent ones, thereby unfolding the full potential of the Connected Metrology® approach. During epitaxy, EpiCurve® TT can determine the thicknesses and composition of many individual layers as well as their radial distribution in-situ. In the ex-situ wafer mapping with EpiX® C2C by white light reflectance and photoluminescence, full 2D wafer maps are acquired characterizing the 2D uniformity of critical layer thickness, layer composition and other sample properties. During sub-sequent plasma-etching processes, the thickness monitoring and endpoint detection is again performed in-situ by LayTec's TRIton®. As the wafer is advancing through the frontend production line, the amount of information on the particular wafer increases and is combined for improved analysis in downstream processes. By connecting in-situ and ex-situ metrology, we can determine the critical layer parameters of increasingly complex layer structures at die-level.

Connected Metrology®

About us

LayTec, founded 1999 in Berlin, is a major provider of in-situ and in-line optical metrology for thin-film processes.

These metrology tools are used in a broad range of thin-film applications such as LED & laser production, power devices and transistors, thin-film photovoltaics, oxide and organic deposition as well as other large area deposition processes. LayTec’s integrated metrology provides access to all key thin-film parameters in real-time – either in-situ, during the deposition process, or in-line. Also, in-situ metrology tools for dry etching have been added expanding LayTec’s portfolio along the production chain.

Beyond these integrated methods, LayTec also offers mapping solutions which ideally complement in-situ measurements by providing uniformity analysis of the deposited layers. The implementation of LayTec metrology systems in production processes significantly shortens development cycles and enables an efficient quality control that helps to considerably reduce production and development costs.

For more information, reach out to **info@laytec.de** or visit **www.laytec.de**.